In class midterm review

Interrupt mode

What interrupt mode is the PIC32MZ in when it first powers up?

**Compatibility mode**

What register bit settings have to be changed and to what values for the PIC32MZ core to switch to EIC mode?

Cause.IV = 1 status.BEV = 0 INTCTL.VS != 0 config.veic = 1

Interrupts

Assume that a PIC32 processor is in EIC multi-vector mode, that the Ebase register currently contains 0x9FC0.1000 and that Intctl.VS = 0x04. If computed offsets are used at what address must the first instruction of the service routine for vector 27 stored?

Ebase + 0x200 + intctl.vs << 5 \* vector #

= 0x9FC0.1F80

If variable offsets are used instead, and what we wanted the address of the first instruction of the service routine for vector 27 to be the same as you found in part a what would have to be done?

Ebase + vector offset

Off027 = F80

Why will an interrupt whose group priority is 0 never be serviced?

Since to interrupt we need the interrupt priority to be greater than the processors current priority level which 0 can never be greater than anything.

Assume that a PIC32MZ processor is properly configured for EIC mode what other register bit settings are required for an interrupt to be serviced?

IE = 1 ERL = 0 EXL = 0 RIPL > IPL, OFFx reg needs to be set up

What role does the sub priority and the IRQ natural order play in deciding which several simultaneous interrupt requests will be served?

It decides which one gets processed first. For group and sub priority bigger is higher priority with IRQ lower is higher priority.

Can an interrupt with group priority 3 and sub-priority 2 interrupt a service routine with group priority 3 and sub-priority 1? Why and why not?

No because sub-priority is not tracked for interrupting only decided with simultaneous interrupts.

Assume a PIC32 processor is in EIC mode, that the Ebase register currently contains 0x9FC0.1000 and that intctl.vS = 0x04

0xBFC0.0000

What is the address of the service routine for an overflow exception?

0x9FC0.1180

What is the address of the service routine for a Reserved Instruction?

0x9FCO.1180